Fig.1

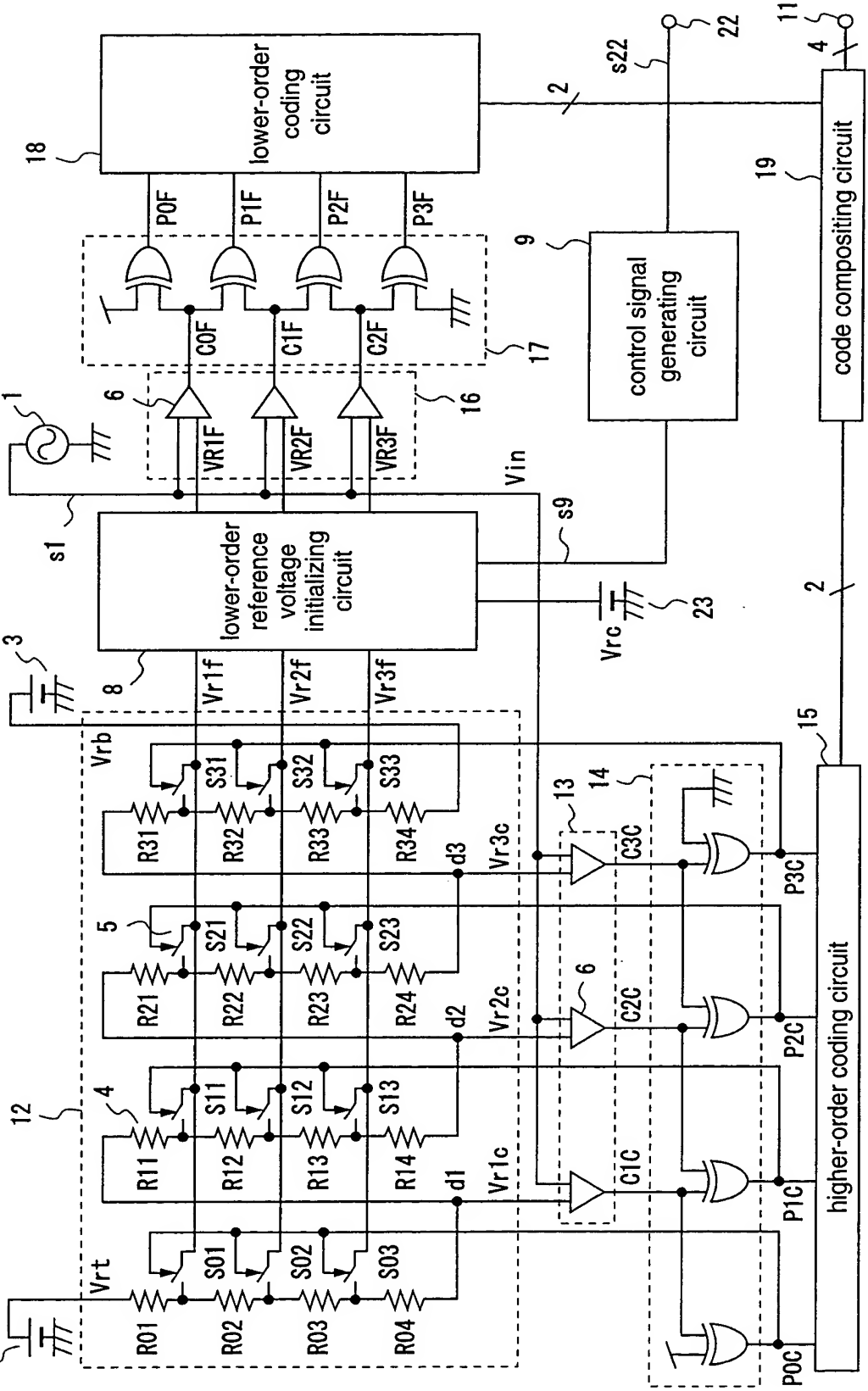

lower-order coding circuit
18
P0F
P1F
P2F
P3F
C0F
C1F
C2F
17
16
VR1F
VR2F
VR3F
6
1
s1
lower-order reference voltage initializing circuit
8
Vin
s9
control signal generating circuit
9
s22
22
11
4
code compositing circuit
19
2
23
Vrc
3
Vr1f
Vr2f
Vr3f
Vrb
Vrt
S31
S32
S33
S21
S22
S23
S11
S12
S13
S01
S02
S03
R31
R32
R33
R34
R21
R22
R23
R24
R11
R12
R13
R14
R01
R02
R03
R04
5
4
12
d3
d2
d1
Vr3c
Vr2c
Vr1c
13
14
C3C
C2C
C1C
P3C
P2C
P1C
P0C
15
higher-order coding circuit

Fig.2

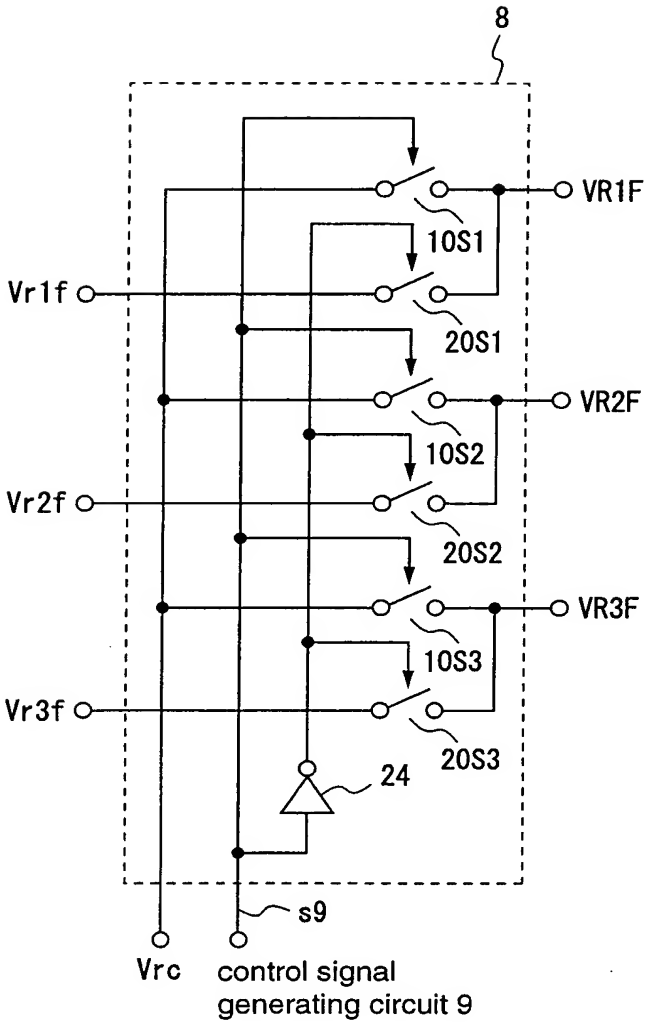
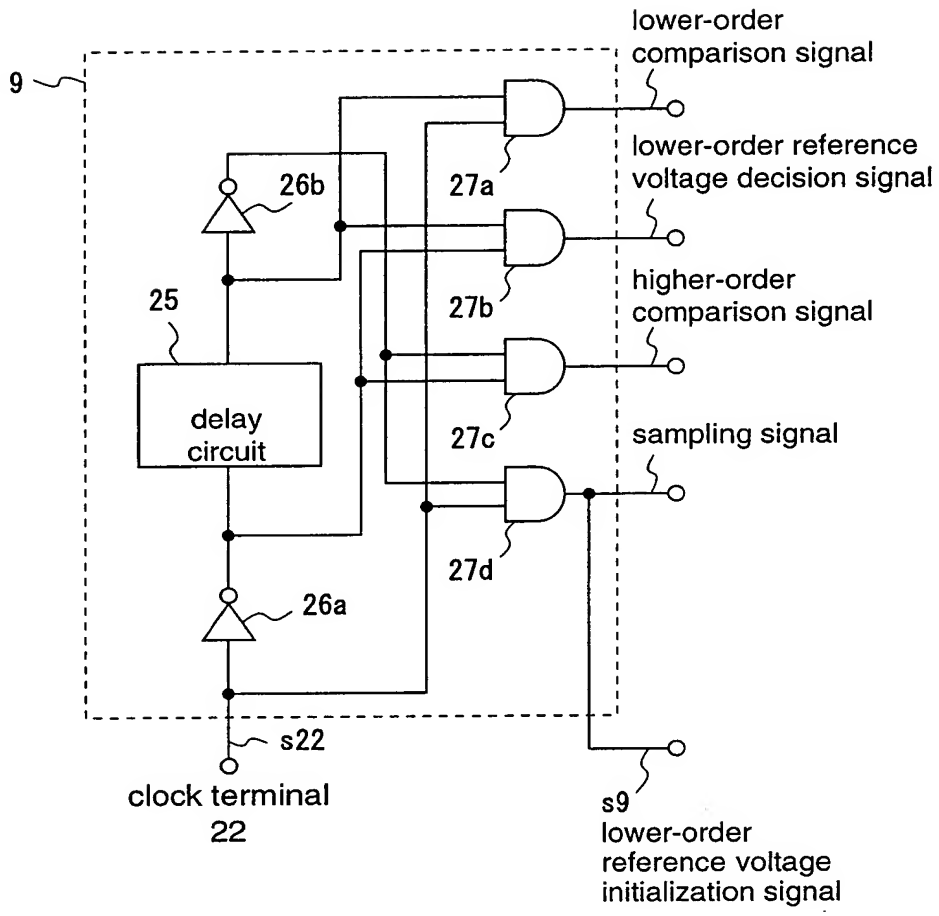

8
VR1F
10S1
Vr1f
20S1
VR2F
10S2
Vr2f
20S2
VR3F
10S3
Vr3f
20S3
24
s9
Vrc
control signal
generating circuit 9

Fig.3


9
lower-order comparison signal
lower-order reference voltage decision signal
higher-order comparison signal
sampling signal
26b
27a
27b
27c
27d
25
delay circuit
26a
s22
clock terminal 22
s9
lower-order reference voltage initialization signal

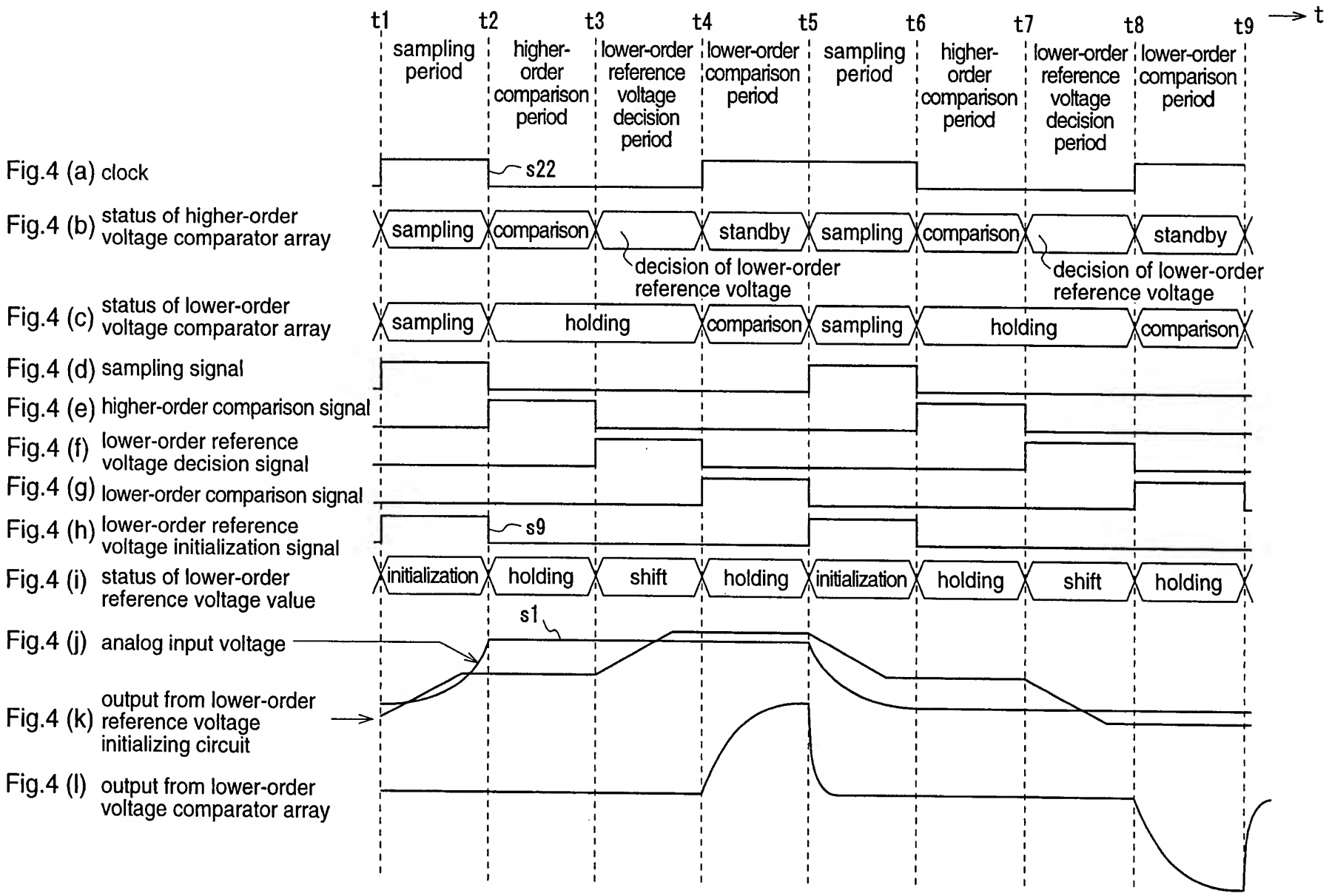

t1
t2
t3
t4
t5
t6
t7
t8
t9
t
sampling period
higher-order comparison period
lower-order reference voltage decision period
lower-order comparison period
sampling period
higher-order comparison period
lower-order reference voltage decision period
lower-order comparison period
Fig.4 (a) clock
s22
Fig.4 (b) status of higher-order voltage comparator array
sampling
comparison
standby
sampling
comparison
standby
decision of lower-order reference voltage
decision of lower-order reference voltage
Fig.4 (c) status of lower-order voltage comparator array
sampling
holding
comparison
sampling
holding
comparison
Fig.4 (d) sampling signal
Fig.4 (e) higher-order comparison signal
Fig.4 (f) lower-order reference voltage decision signal
Fig.4 (g) lower-order comparison signal
Fig.4 (h) lower-order reference voltage initialization signal
s9
Fig.4 (i) status of lower-order reference voltage value
initialization
holding
shift
holding
initialization
holding
shift
holding
s1
Fig.4 (j) analog input voltage
Fig.4 (k) output from lower-order reference voltage initializing circuit
Fig.4 (l) output from lower-order voltage comparator array

Fig.5

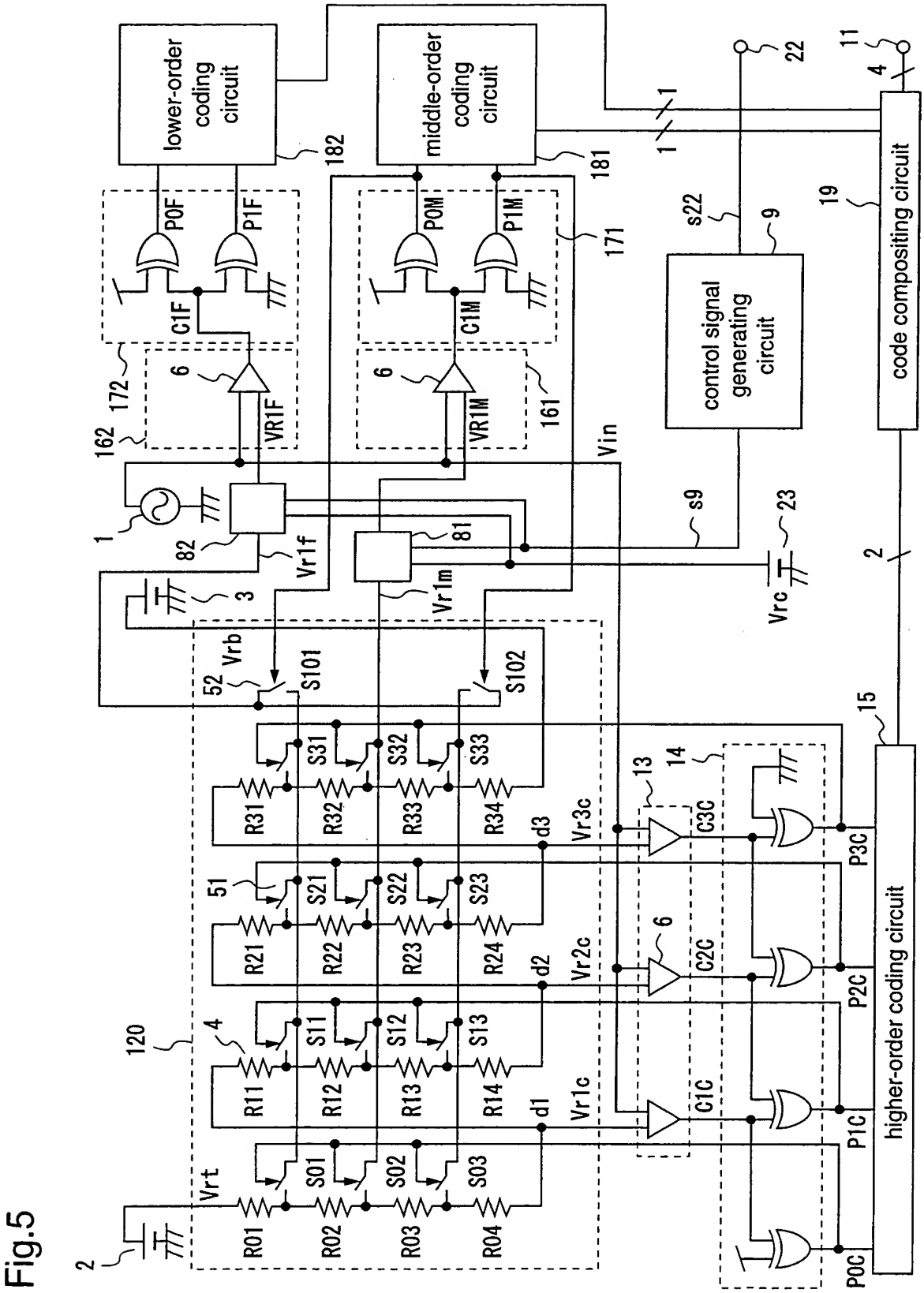

lower-order coding circuit
middle-order coding circuit
control signal generating circuit
code compositing circuit
higher-order coding circuit
P0F
P1F
P0M
P1M
C1F
C1M
VR1F
VR1M
Vin
Vr1f
Vr1m
Vrc
Vrb
Vrt
S101
S102
R01
R02
R03
R04
R11
R12
R13
R14
R21
R22
R23
R24
R31
R32
R33
R34
S01
S02
S03
S11
S12
S13
S21
S22
S23
S31
S32
S33
d1
d2
d3
Vr1c
Vr2c
Vr3c
C1C
C2C
C3C
P0C
P1C
P2C
P3C
s9
s22
120
172
182
181
171
161
162

Fig.6

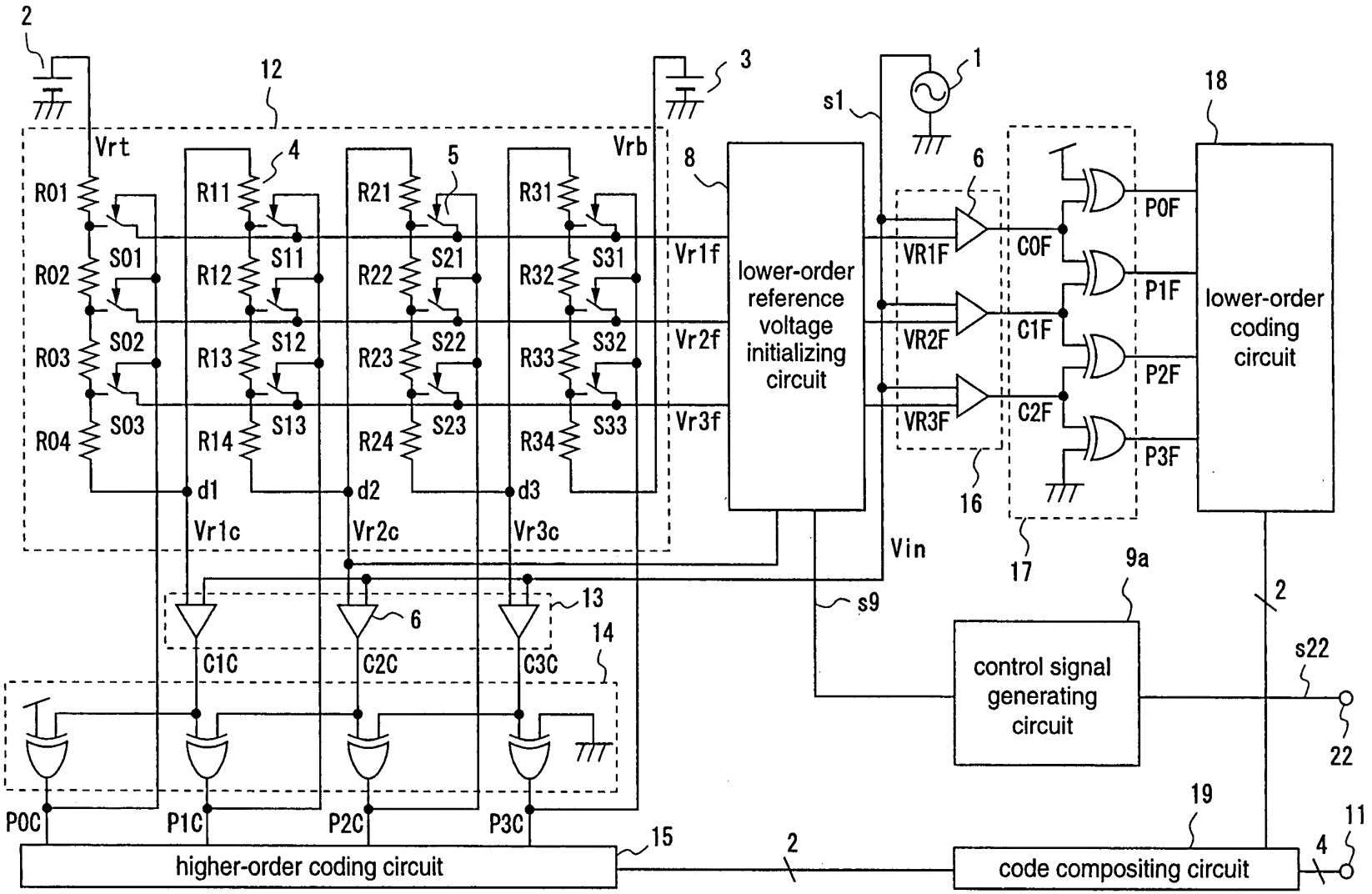
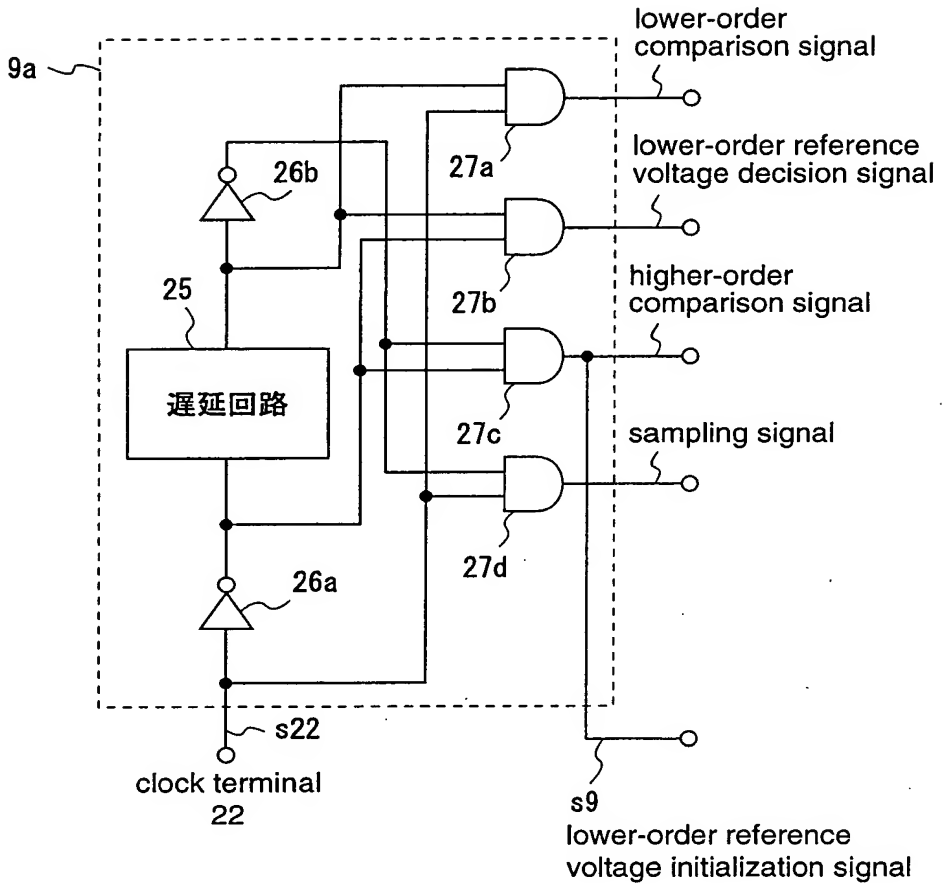

2
12
3
1
s1
18
Vrt
Vrb
4
5
8
6
R01
R11
R21
R31
S01
S11
S21
S31
R02
R12
R22
R32
Vr1f
lower-order reference voltage initializing circuit
VR1F
C0F
P0F
P1F
lower-order coding circuit
S02
S12
S22
S32
R03
R13
R23
R33
Vr2f
VR2F
C1F
P2F
S03
S13
S23
S33
R04
R14
R24
R34
Vr3f
VR3F
C2F
P3F
d1
d2
d3
16
Vr1c
Vr2c
Vr3c
Vin
17
9a
2
13
6
s9
14
C1C
C2C
C3C
control signal generating circuit
s22
22
P0C
P1C
P2C
P3C
19
11
15
2
4
higher-order coding circuit
code compositing circuit

Fig.7


9a
lower-order
comparison signal
lower-order reference
voltage decision signal
higher-order
comparison signal
sampling signal
26b
27a
27b
27c
27d
25
遅延回路
26a
s22
clock terminal
22
s9
lower-order reference
voltage initialization signal

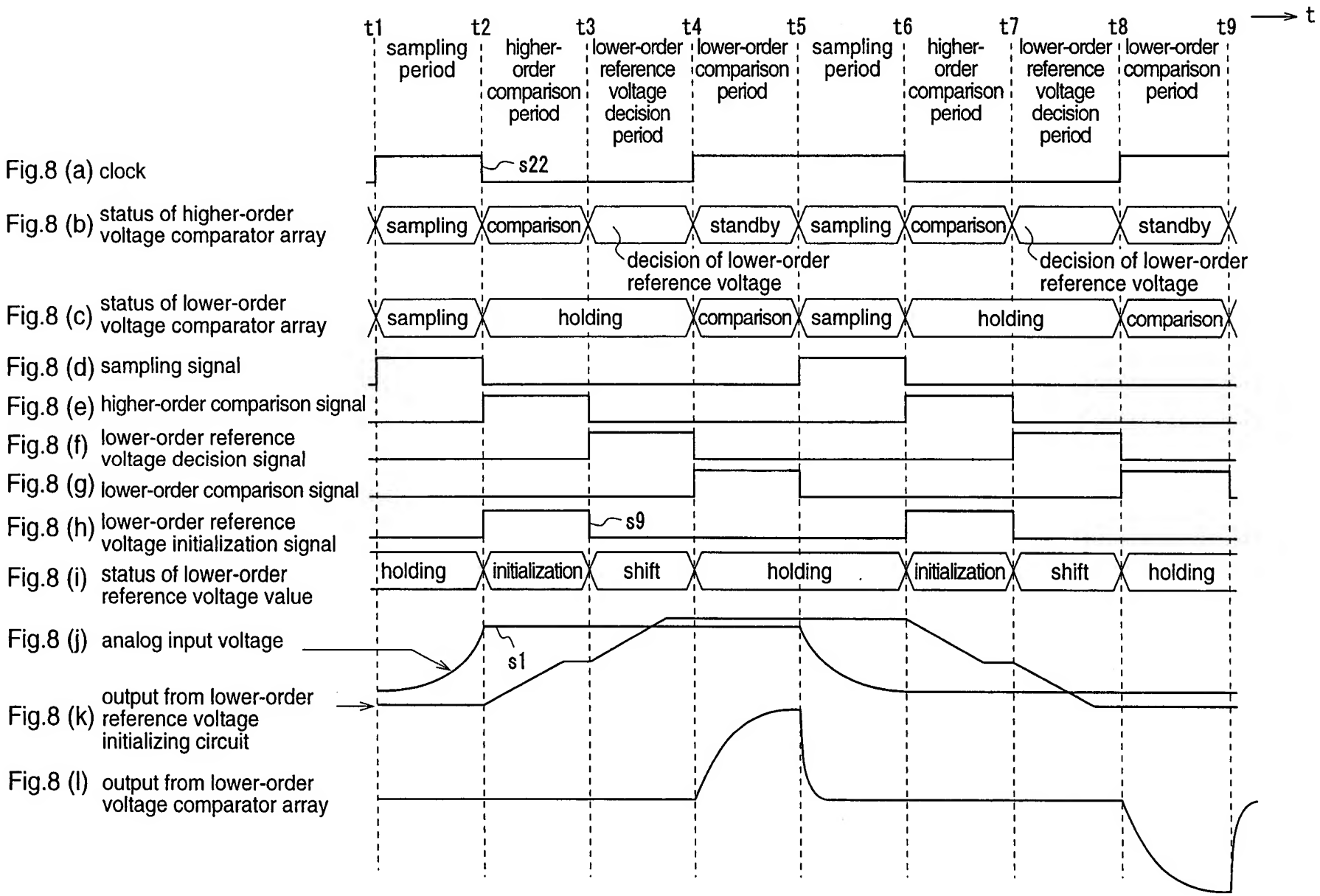

t1
t2
t3
t4
t5
t6
t7
t8
t9
t
sampling period
higher-order comparison period
lower-order reference voltage decision period
lower-order comparison period
sampling period
higher-order comparison period
lower-order reference voltage decision period
lower-order comparison period
Fig.8 (a) clock
s22
Fig.8 (b) status of higher-order voltage comparator array
sampling
comparison
standby
sampling
comparison
standby
decision of lower-order reference voltage
decision of lower-order reference voltage
Fig.8 (c) status of lower-order voltage comparator array
sampling
holding
comparison
sampling
holding
comparison
Fig.8 (d) sampling signal
Fig.8 (e) higher-order comparison signal
Fig.8 (f) lower-order reference voltage decision signal
Fig.8 (g) lower-order comparison signal
Fig.8 (h) lower-order reference voltage initialization signal
s9
Fig.8 (i) status of lower-order reference voltage value
holding
initialization
shift
holding
initialization
shift
holding
Fig.8 (j) analog input voltage
s1
Fig.8 (k) output from lower-order reference voltage initializing circuit
Fig.8 (l) output from lower-order voltage comparator array

Fig.9

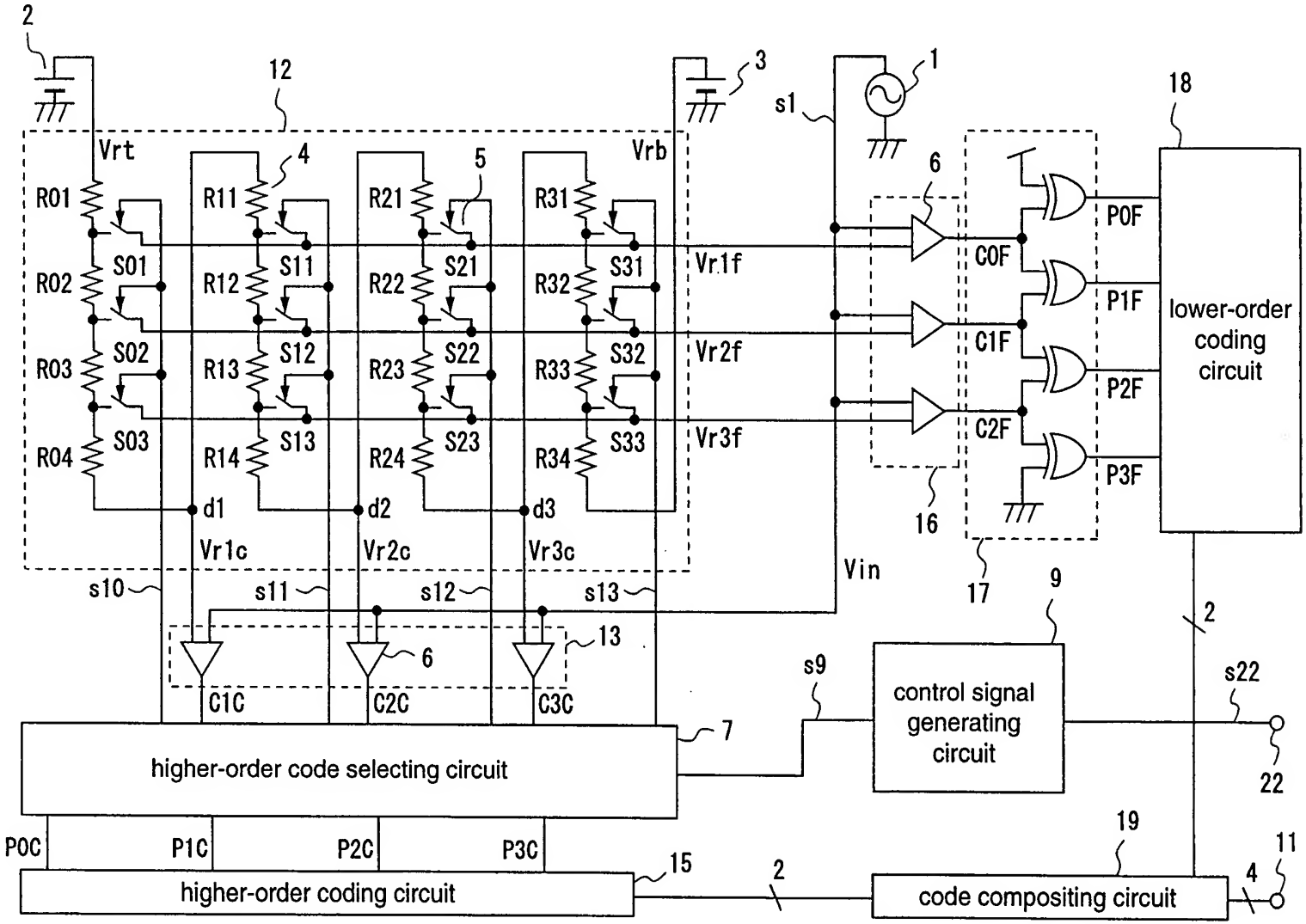
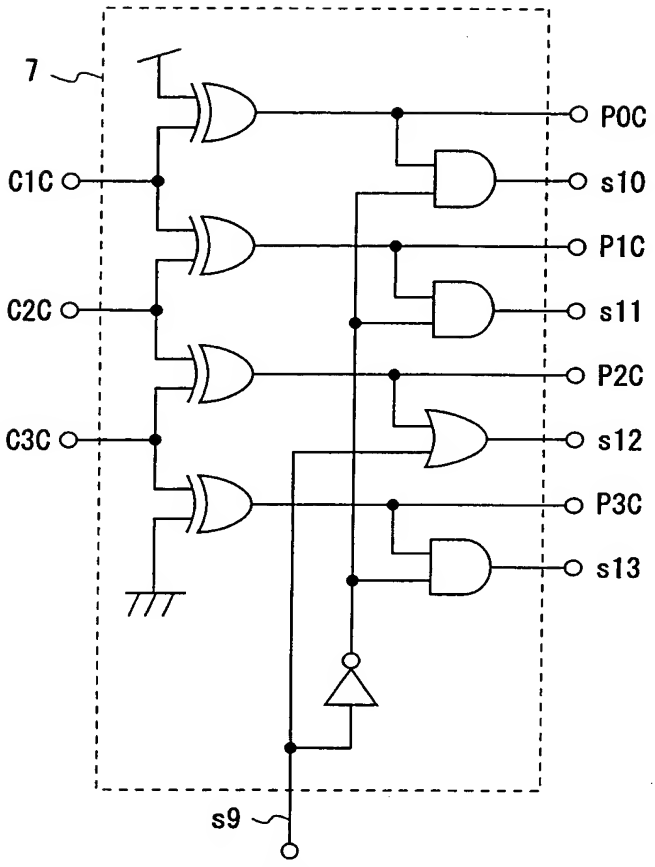

2
12
3
1
s1
18
Vrt
Vrb
4
5
6
R01
R11
R21
R31
S01
S11
S21
S31
R02
R12
R22
R32
Vr1f
S02
S12
S22
S32
R03
R13
R23
R33
Vr2f
S03
S13
S23
S33
R04
R14
R24
R34
Vr3f
C0F
C1F
C2F
P0F
P1F
P2F
P3F
lower-order coding circuit
d1
d2
d3
Vr1c
Vr2c
Vr3c
16
17
Vin
9
s10
s11
s12
s13
13
6
C1C
C2C
C3C
2
s9
control signal generating circuit
s22
7
higher-order code selecting circuit
22
19
P0C
P1C
P2C
P3C
11
15
2
4
higher-order coding circuit
code compositing circuit

Fig.10


7
C1C
C2C
C3C
P0C
s10
P1C
s11
P2C
s12
P3C
s13
s9
control signal
generating circuit 9

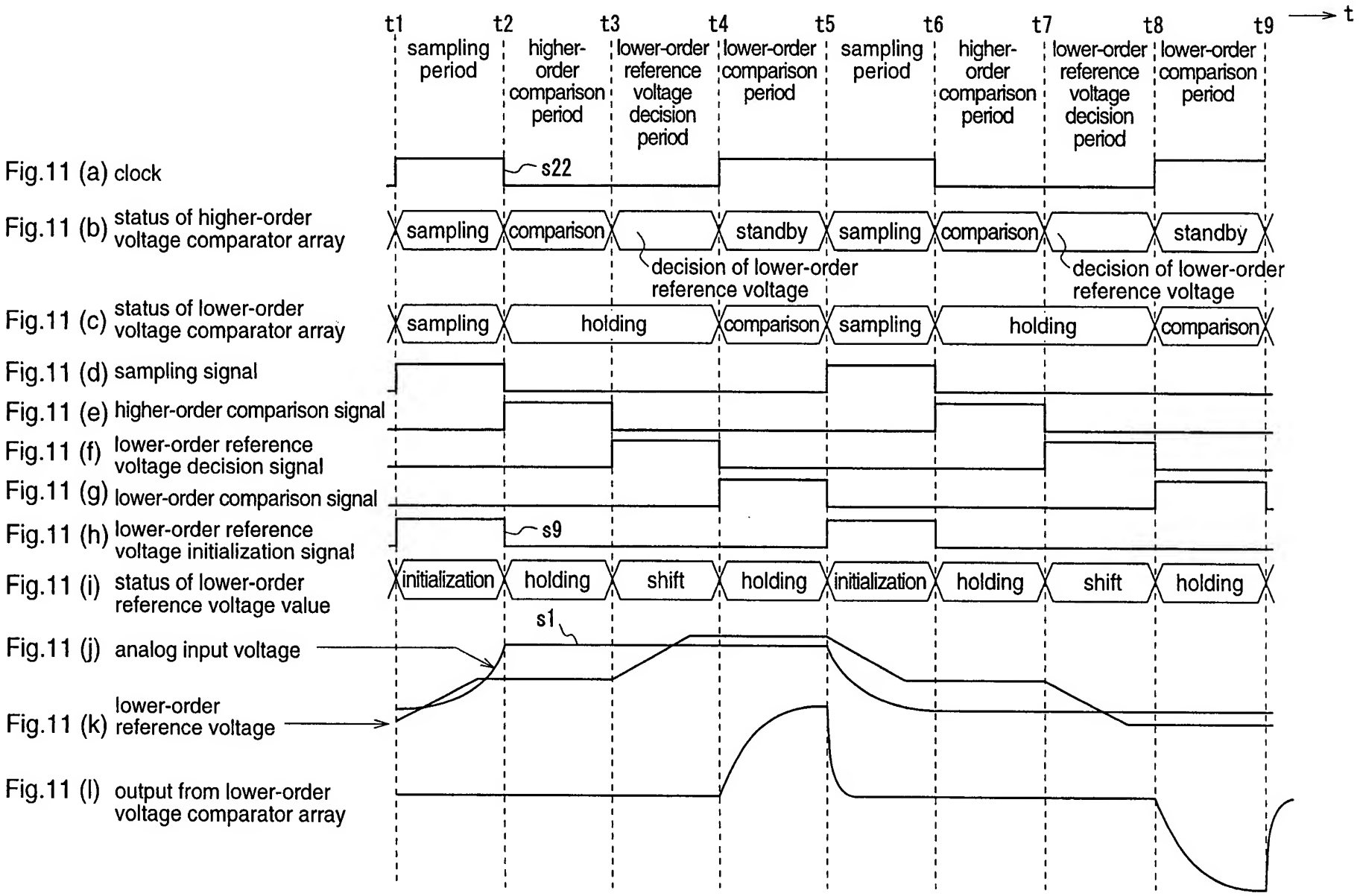
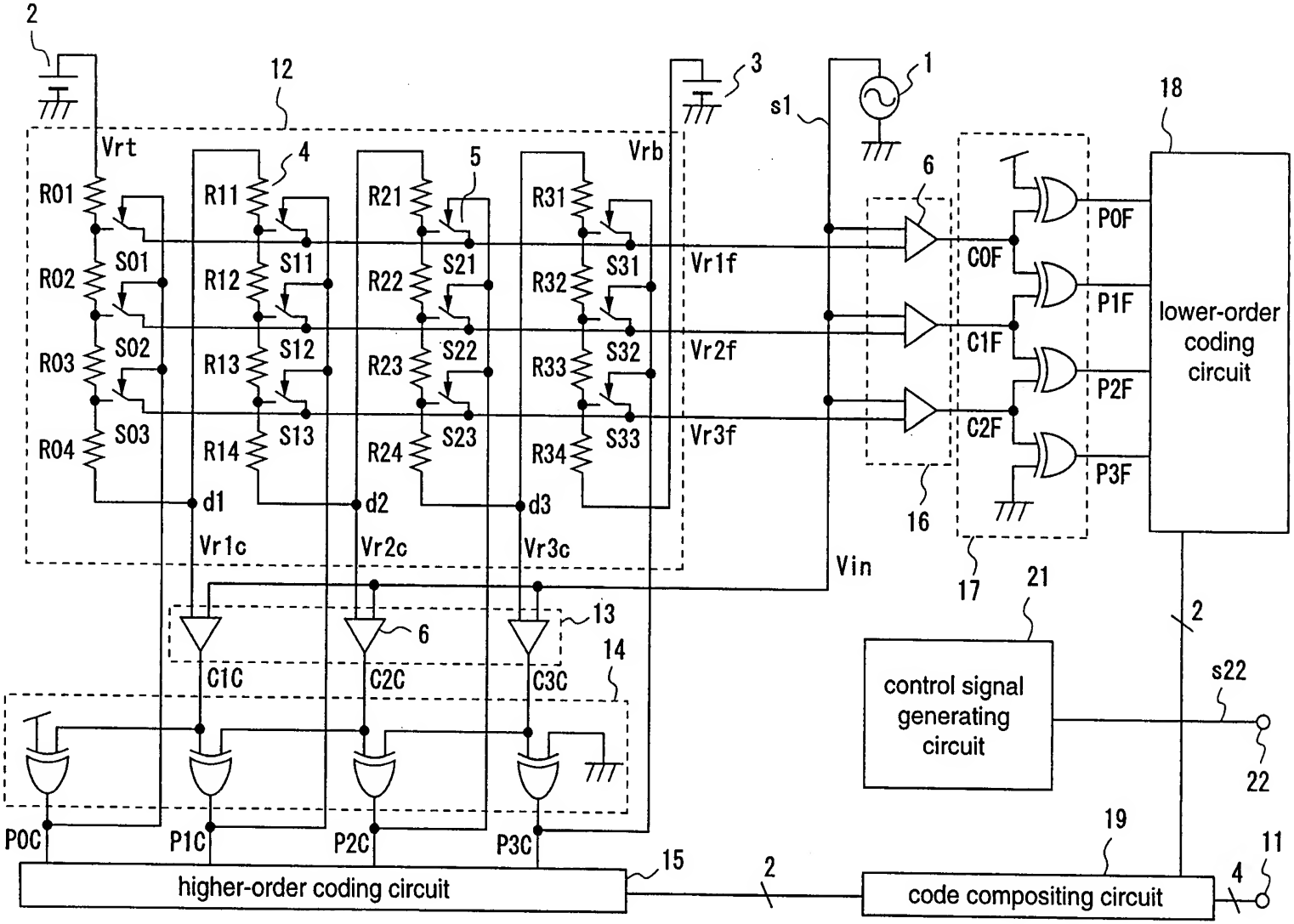
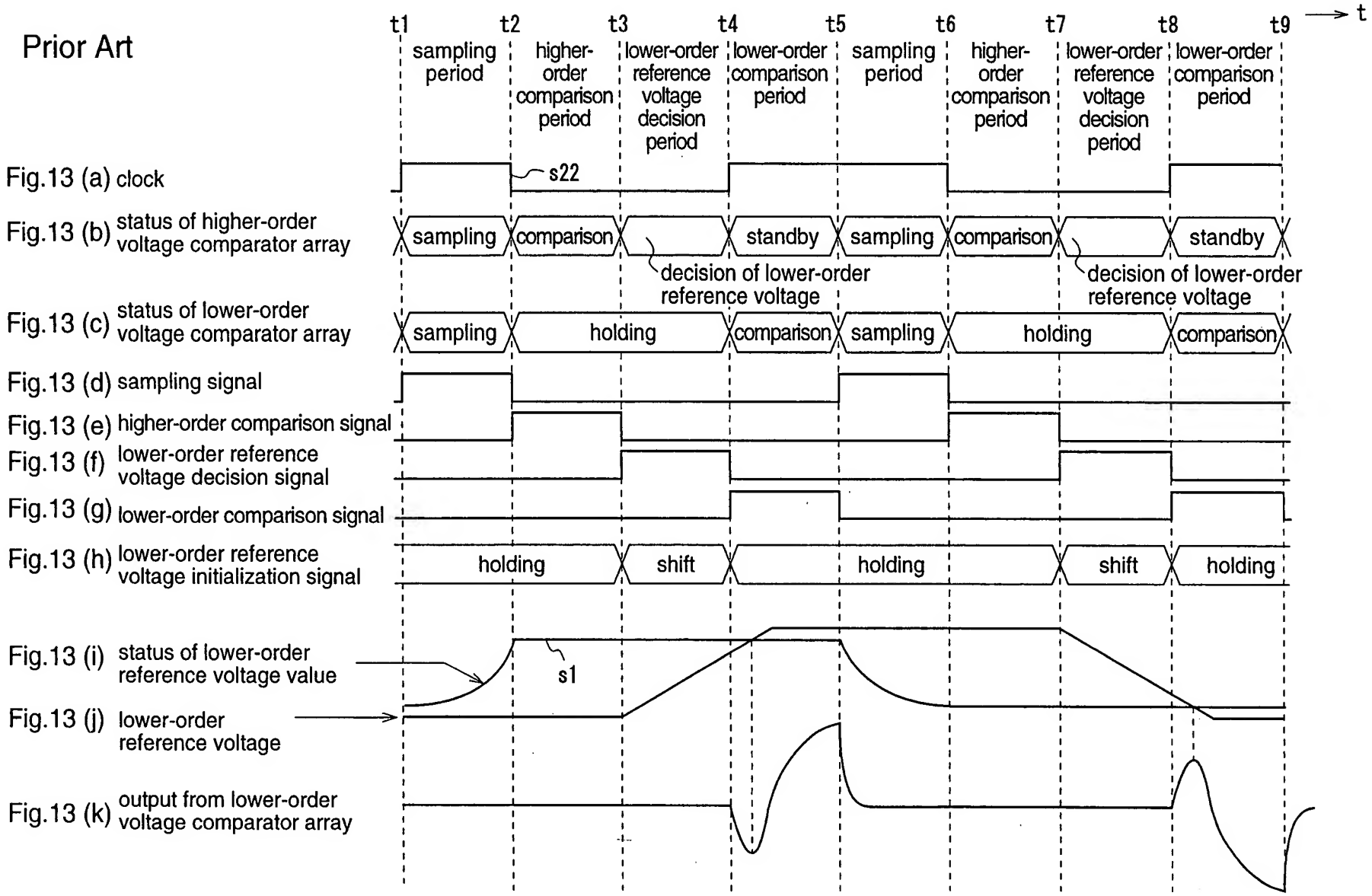

t1
t2
t3
t4
t5
t6
t7
t8
t9
t
sampling period
higher-order comparison period
lower-order reference voltage decision period
lower-order comparison period
sampling period
higher-order comparison period
lower-order reference voltage decision period
lower-order comparison period
Fig.11 (a) clock
s22
Fig.11 (b) status of higher-order voltage comparator array
sampling
comparison
standby
sampling
comparison
standby
decision of lower-order reference voltage
decision of lower-order reference voltage
Fig.11 (c) status of lower-order voltage comparator array
sampling
holding
comparison
sampling
holding
comparison
Fig.11 (d) sampling signal
Fig.11 (e) higher-order comparison signal
Fig.11 (f) lower-order reference voltage decision signal
Fig.11 (g) lower-order comparison signal
Fig.11 (h) lower-order reference voltage initialization signal
s9
Fig.11 (i) status of lower-order reference voltage value
initialization
holding
shift
holding
initialization
holding
shift
holding
s1
Fig.11 (j) analog input voltage
Fig.11 (k) lower-order reference voltage
Fig.11 (l) output from lower-order voltage comparator array

Fig.12 Prior Art



Prior Art


t1
t2
t3
t4
t5
t6
t7
t8
t9
t
sampling period
higher-order comparison period
lower-order reference voltage decision period
lower-order comparison period
sampling period
higher-order comparison period
lower-order reference voltage decision period
lower-order comparison period
Fig.13 (a) clock
s22
Fig.13 (b) status of higher-order voltage comparator array
sampling
comparison
standby
sampling
comparison
standby
decision of lower-order reference voltage
decision of lower-order reference voltage
Fig.13 (c) status of lower-order voltage comparator array
sampling
holding
comparison
sampling
holding
comparison
Fig.13 (d) sampling signal
Fig.13 (e) higher-order comparison signal
Fig.13 (f) lower-order reference voltage decision signal
Fig.13 (g) lower-order comparison signal
Fig.13 (h) lower-order reference voltage initialization signal
holding
shift
holding
shift
holding
Fig.13 (i) status of lower-order reference voltage value
s1
Fig.13 (j) lower-order reference voltage
Fig.13 (k) output from lower-order voltage comparator array